LISTING OF CLAIMS

1. (Currently Amended) A stream routing unit for routing each of a plurality of input packet streams to any of a plurality of destinations, the stream routing unit comprising:

a plurality of input ports for receiving respective input streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at arbitrarily addressable locations each identifiable by an address;

an assignment data structure identifying for each source of the input packet stream at least one destination to which each input packet stream is to be routed; ~~and~~

a packet allocation table comprising an array including a plurality of slots ~~data structure~~ holding for each new incoming packet a source identifier identifying the source ~~origin~~ of the packet and the arbitrary address in the storage means where the packet is held, the packet allocation table ~~data structure~~ further ~~holding~~ including a plurality of destination pointers, each destination pointer associated with one of the output ports, each destination pointer being assignable to any slot so as to identify ~~information identifying~~ the output ports associated with the intended destinations of a held packet, the assigning of each destination pointer to a slot ~~information~~ being derived using ~~from~~ the assignment data structure; and

processing means for controlling the removal of packets from the storage means to the plurality of output ports using the destination pointers.

2. (Original) The stream routing unit according to claim 1, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

3. (Previously Presented) The stream routing unit according to claim 1, wherein the assignment data structure is a data matrix.

4. (Canceled).

5. (Currently Amended) The stream routing unit according to claim 1 [[4]], wherein the packet allocation table ~~data structure~~ is associated with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

6. (Canceled).

7. (Original) The stream routing unit according to claim 1, wherein the packets of a said input stream are of a common length.

8. (Currently Amended) A data communication system for routing incoming packets to at least one destination, the system comprising:

a plurality of packet stream sources each generating a packet stream;

a stream routing unit comprising:

a plurality of input ports for receiving respective input packet streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at arbitrarily addressable locations each identifiable by an address;

an assignment data structure identifying for each source of the input packet stream at least one destination to which each input packet stream is to be routed; ~~and~~

a packet allocation table comprising an array including a plurality of slots ~~data structure~~ holding for each new incoming packet a source identifier identifying the source ~~origin~~ of the packet and the arbitrary address in the storage means where the packet is held, the packet allocation table ~~data structure~~ further ~~holding~~ including a plurality of destination pointers, each destination pointer associated with one of the output ports, each destination pointer being assignable to any slot so as to identify ~~information identifying~~ the output ports associated with the intended destinations of a held packet, the assigning of each destination pointer to a slot ~~information~~ being derived using ~~from~~ the assignment data structure; and

processing means for controlling the removal of packets from the storage means to the plurality of output ports using the destination pointers; and

a plurality of destinations for receiving packets of the packet streams generated by the sources.

9. (Original) The data communication system according to claim 8, wherein at least one of the destinations comprises a programmable transport interface.

10. (Original) The data communication system according to claim 8, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

11. (Currently Amended) A method of routing packet streams from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams;

identifying for each source of the input packet stream at least one destination to which each input packet stream is to be routed using an assignment data structure;

holding each packet of the packet stream in a storage means at an arbitrarily addressable location identifiable by an address in that storage means;

holding for each new incoming packet a packet allocation table comprising an array including a plurality of slots ~~data structure~~ which stores a source identifier identifying the source ~~origin~~ of the packet and the arbitrary address in the storage means where the packet is held;

holding information in an assignment data structure identifying for each source at least one ~~the~~ intended destination of the packet ~~derived from the assignment data structure~~;

providing a plurality of destination pointers, each destination pointer associated with an output port for one of the destinations, each destination pointer being assignable to any slot so as to identify the output ports associated with the intended destinations of a held packet;

using said assignment data structure information identifying the intended destination from the packet source to assign each destination pointer to a slot of the packet allocation table ~~further include in the packet allocation data structure information identifying output ports associated with intended destinations of a held packet~~;

retrieving the packet from the memory means at the arbitrary address contained in the slot to which each destination pointer is assigned; and

routing the addressed packet from the storage means to the or each output port associated with the respective destination pointer(s) ~~identified destination(s)~~.

12. (Original) The method according to claim 11, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the output ports.

13. (Canceled).

14. (Currently Amended) The method according to claim 11 further comprising: ~~holding each new incoming packet in a packet allocation data structure having a plurality of slots; holding in each slot a source identifier and associated address; and~~

associating each slot with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

15. (Currently Amended) A device for delivering incoming packets to at least one destination, the device comprising:

an addressable memory which stores incoming packets at a plurality of address locations in the memory;

a source to destination matrix for mapping at least one source to at least one destination;

a packet allocation table including a plurality of slots, each slot ~~for~~ associating a source ~~and at least one destination~~ for a particular packet with the address location in the addressable memory where the particular packet is stored;

a plurality of destination pointers associated with the packet allocation table, each destination pointer having an associated destination, and each destination pointer being assignable to any slot in the packet allocation table; and

an algorithm for controlling removal of the incoming packets from a memory to at least one destination, the algorithm assigning each destination pointer to a slot in the packet allocation table based on the source and destination information within the source to destination matrix, wherein the packet at the address location within the slot of the packet allocation table assigned to the destination pointer is retrieved from the addressable memory and ~~incoming packets have a lower bit rate than packets~~ delivered to the at least one destination.

16. (Original) The device of claim 15 further comprising a memory for holding the incoming packets at addressable locations each identifiable by an address.

17. (Original) The device of claim 15 further comprising:

a plurality of input ports for receiving respective input packets; and

a plurality of output ports associated with respective destinations to which the input packets can be routed.

Claims 18-31. (Canceled).

32. (Previously Presented) The stream routing unit according to claim 6, wherein the destination pointers are assigned by an algorithm.

33. (Previously Presented) The stream routing unit according to claim 32, wherein after the assignment of destination pointers is completed, the algorithm controls the storage means to output a packet according to the status of the destination pointers.

34. (Previously Presented) The stream routing unit according to claim 1, wherein held packets are output in the order in which they are received.

35. (Previously Presented) The stream routing unit according to claim 1, further comprising means for outputting the held packet only when all of the output ports associated with the intended destinations of the held packet are free.

36. (Currently Amended) A stream routing unit, comprising:

a plurality of input ports, each input port receiving an input packet stream;

a plurality of output ports, each output port outputting an output packet stream;

a memory including a plurality of addressable memory locations;

a source-to-destination matrix mapping ~~storing data identifying, for~~ each source of the input packet streams coupled to the input ports to [[,]] one or more destinations, for packets within those input packet streams, which are coupled to receive the output packet streams from the output ports;

a processor for storing packets of the input packet streams in the memory and for retrieving stored packets from the memory to form the output packet streams;

the processor filling a packet allocation table which includes a plurality of slot locations, each slot location storing a source identifier which identifies a source of the received packet stream to which a given packet belongs linked in the slot of the packet allocation table to an address in the memory for the addressable memory location where that given packet has been stored by the processor;

a destination pointer, associated with each one of the output ports, implemented by the processor for pointing to a slot location in the packet allocation table from which the address of the given packet is retrieved, the destination pointer pointing to the slot location when the source identifier in the slot is associated with a source that is mapped through ~~in accordance with the destination data stored in~~ the source-to-destination matrix to a destination coupled to an output port and that output port is associated with that destination pointer;

the processor retrieving the given packet from the memory at the address provided in the slot location pointed at by the destination pointer, sending the retrieved given packet to each output port associated with that destination pointer ~~the destination that is linked in the source-to-destination matrix with the source identified in the slot location~~ for inclusion in the output packet stream of the output port.

37. (Previously Presented) The stream routing unit of claim 36 further comprising a write pointer implemented by the processing means for pointing to an open slot location in the packet allocation table to which the source identifier and address of the given packet are written.

38. (Previously Presented) The stream routing unit of claim 36, wherein a bit rate of the input packet streams is lower than a bit rate of the output packet streams.